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(54) **Method of manufacturing a gate electrode**

(57) The present invention provides a semiconductor device and a method of manufacturing the same improved in reliability of a gate insulating film (122) by increasing a total charge amount Qbd by suppressing a film stress of a gate electrode (123a) formed of a polysilicon film (123), to a low value. Since the film stress is closely related to a film formation temperature, it is possible to reduce the film stress lower than the conventional case by forming a film at as a high temperature as 640°C or more. At this time, when the film stress decreases, the total charge amount Qbd regulating dielectric breakdown of the film (122) increases, improving reliability of the gate insulating film (122). It is therefore possible to set the film stress of the gate electrode (123a) at 200 MPA or less in terms of absolute value by forming the gate electrode (123a) at 640°C or more.

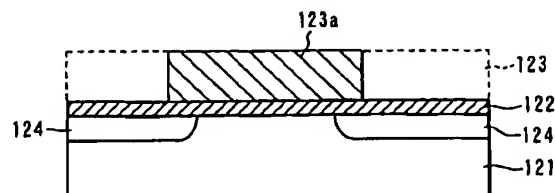


FIG. 2

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Description

[0001] The present invention relates to a semiconductor device constituted of an integrated circuit having a MOS transistor formed therein, and more particularly, to a method of forming a gate electrode for improving reliability of a gate insulating film of the MOS transistor.

[0002] Now, we will explain steps of manufacturing the MOS transistor which serves as a constitutional element of an integrated circuit formed on a conventional semiconductor substrate, by taking an NMOS transistor having an LDD (lightly doped drain) structure, as an example. First, an element isolating region 2 is formed on a surface region of a p-type silicon semiconductor substrate 1 by a LOCOS method or the like. A gate insulating film (SiO_2) 3 is formed on an element region surrounded by the element isolating region 2. Then, boron ions are injected (channel ion injection) over an entire main surface of the semiconductor substrate 1 to control a threshold voltage (FIG. 9A). Subsequently, a polysilicon film is deposited over the entire main surface of the semiconductor substrate 1 and patterned to form a gate electrode 4 of polysilicon (PolySi) on the gate insulating film 3 in the element region. Thereafter, P (phosphorus) ions are injected in a low amount to form an n⁺ source/drain region 5 for mitigating a high electric field (FIG. 9B).

[0003] Next, a silicon oxide film (SiO_2) 6 is deposited on the semiconductor substrate 1 by a CVD (Chemical Vapor Deposition) method or the like so as to cover the gate electrode 4 (FIG. 10A). Subsequently, the silicon oxide film 6 is anisotropically etched to form a side wall insulating film 7 on a side wall of the gate electrode 4. Thereafter, n-type impurity ions such as arsenic (As) ions are doped in a high amount to form an n⁺ source/drain region 8 (FIG. 10B).

[0004] As described above, in the MOS transistor, a polysilicon film doped with phosphorus, arsenic, or boron is generally used as the gate electrode. The polysilicon film is deposited by an LPCVD method at a reaction-chamber ambient temperature of about 600°C. The polysilicon film deposited under the aforementioned conditions has a film stress of 300 MPa or more despite the presence or absence of a dopant. Such a high stress of the gate electrode is applied to a gate insulating film (in this prior art, the film may be composed of a silicon oxide film, hereinafter simply called "gate insulating film", for the simplicity of explanation) whereby the high stress affects reliability of the gate insulating film or gate insulating film formed under the gate electrode. To explain more specifically, when the stress is applied to the gate insulating film, the bonding between silicon and oxygen constituting the gate insulating film is distorted. As a result, the bonding is tend to be easily broken, readily inducing dielectric breakdown of the gate insulating film.

[0005] When intrinsic dielectric breakdown of the insulating film takes place, the total amount Qbd of elec-

tric charge passing through the insulating film is up to about 15 C/cm² under application of an electric field of 12 MV/cm to the insulating film, assuming that the thickness of the insulating film is about 10 nm. The total charge amount Qbd is a value on the basis of which the reliability of a transistor is determined. Therefore, the Qbd desirably has a large value. Particularly, in non-volatile storage device, such as EEPROM (Electrically Erasable Programmable Read Only memory) in which data is written into a memory cell by using a tunnel current, how many times can be programmed is restricted by the total charge amount Qbd. Therefore, it is necessary to increase the total charge amount Qbd in order to improve performance of the device.

[0006] The present invention was made in view of the aforementioned circumstances. The present invention provides a semiconductor device and a method of manufacturing the same, improved in reliability of a gate insulating film and increased in its total charge amount Qbd by suppressing a film stress of a gate electrode formed of a polysilicon film, to a low value.

[0007] Since the film stress of a gate electrode is closely related with a film formation temperature, it is possible to reduce the film stress lower than in the conventional case, by forming a film at as a high temperature as 640°C or more, preferably 650°C or more. With a decrease in the film stress of the gate electrode at this time, the total charge amount Qbd of a gate insulating film underlying the gate electrode increases, with the result that reliability not only of the gate insulating film but also a semiconductor device including the gate insulating film is improved.

[0008] More specifically, the semiconductor device of the present invention comprises

- a semiconductor substrate;
- source/drain regions formed on the semiconductor substrate;
- a gate insulating film formed between the source/drain regions on the semiconductor substrate; and
- a gate electrode formed on the gate insulating film, in which
- a film stress of the gate electrode is 200 MPa or less in terms of absolute value.

[0009] The gate electrode may be a polysilicon film and may be in contact with the gate insulating film.

[0010] A metal silicide film or a high-melting point metal film may be formed on the polysilicon film.

In other words, the gate electrode may be formed of the polysilicon film and the metal silicide film or the high melting point metal film. Furthermore, the high melting point metal film is formed on the metal silicide film, and therefore, the gate electrode may be formed of the polysilicon film, the metal silicide film, and the high melting point metal film.

[0011] A MOS transistor having the source/drain

regions, the gate insulating film, and the gate electrode, may be adopted in a non-volatile semiconductor storage device such as an EEPROM. When the MOS transistor according to the invention is used in an EEPROM, the programmable number can be increased since a total charge amount Qbd of electric charge passing through the gate insulating film serving as a floating gate has a direct effect upon characteristics of a device.

[0012] According to the present invention, there is provided a method of manufacturing a semiconductor device, according to the present invention comprises the steps of:

forming source/drain regions in a semiconductor substrate;

forming a gate insulating film between the source/drain regions on the semiconductor substrate; and

forming a gate electrode including a polysilicon film on the gate insulating film and having a film stress of 200 MPa or less;

in which

the polysilicon film is formed by depositing polysilicon on the gate insulating film by a CVD method at a temperature of 640°C or more. Preferably, the temperature at which a gate insulating film is formed may be 650°C or more, in order to stably provide a gate electrode whose film stress is 200 MPa or less.

[0013] The polysilicon film may be formed while the semiconductor substrate is rotated at a high speed. In this manner, it is possible to form a uniform film on a semiconductor substrate.

[0014] This summary of the invention does not necessarily describe all necessary features so that the invention may also be a sub-combination of these described features.

[0015] The invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a schematic sectional view of a single-wafer processing LPCVD apparatus used in a first embodiment;

FIG. 2 is a cross-sectional view of a semiconductor substrate having a MOS capacitor according to the present invention;

FIG. 3 is a characteristic graph showing the relationship between deposition temperature of a polysilicon film and film stress;

FIGS. 4A and 4B show that a semiconductor substrate is bent by a compression stress or tensile stress generated in a gate electrode (polysilicon film);

FIGS. 5A and 5B are conceptual diagram for explaining how a bent amount is calculated, FIG. 5A relates to the situation prior to the formation of a

polysilicon film on the silicon substrate, and FIG. 5B relates to the situation after the formation of a polysilicon film on the silicon substrate.

FIG. 6 is a characteristic graph showing the relationship between the film stress of the polysilicon film and the total charge amount of a gate insulating film;

FIG. 7 is a schematic sectional view of a single-wafer processing LPCVD apparatus used in a second embodiment;

FIG. 8 is a cross sectional view of EEPROM according to a third embodiment;

FIGS. 9A and 9B are cross sectional views showing manufacturing steps of a semiconductor substrate having a conventional MOS transistor; and

FIGS. 10A and 10B are cross sectional views showing the manufacturing steps of a semiconductor substrate having a conventional MOS transistor.

[0016] Now, embodiments of the present invention will be explained with reference to the accompanying drawings.

[0017] First, referring to FIGS. 1 to 6, a first embodiment will be explained.

[0018] FIG. 1 is a schematic sectional view of a single-wafer processing LPCVD (Low pressure CVD) apparatus. FIG. 2 is a cross sectional view of a MOS capacitor formed on a semiconductor substrate. FIG. 3 is a characteristic graph showing dependency of the film stress (MPa) of the polysilicon film on the semiconductor substrate upon deposition temperature. FIGS. 4A to 5B are conceptual diagram explaining the way of measuring a film stress. FIG. 6 is a characteristics graph showing a total charge amount Qbd (C/cm²) of the gate insulating film.

[0019] As shown in FIG. 1, the LPCVD apparatus has a reaction chamber 13 (hereinafter, referred to as "film formation chamber"). The film-formation chamber 13 is equipped with a susceptor 15 on which a semiconductor wafer 16 is mounted. The inner space of the film formation chamber 13 is heated by a plurality of infrared lamps 14 arranged around the chamber in close proximity thereto, during film formation time. A reactive gas is supplied from a pipe 10 to the inner space of the film formation chamber 13 while being controlled by a mass-flow controller 11 and a valve 12. After completion of a reaction, an exhaust gas is discharged by a pump 112 through a pipe 111. The pump 112 is controlled by a valve 18 and a conductance valve 19 while the pressure is monitored by a pressure gage 17 attached to the pipe 111.

[0020] As shown in FIG. 2, an thermal oxidation film serving as a gate insulating film 122 and formed on a silicon semiconductor substrate 121 is oxidized with O₂, H₂O, or HCl gas at a temperature of 800°C to render the thickness at 8 nm. Thereafter, the semiconductor substrate 121 (semiconductor wafer 16) is placed in the film-formation chamber 13 of the LPCVD apparatus

shown in FIG. 1. Then, a polysilicon film 123 is formed on the semiconductor wafer 16 in a thickness of about 200 nm at a film-formation temperature of 680°C and a pressure of 5 Torr while SiH₄ gas is supplied at a flow rate of 1 SLM and AsH₃ gas at a flow rate of 1 sccm. At this time, the concentration of As in the polysilicon film 123 is about 1×10^{20} atoms/cm³. Thereafter, the polysilicon film 123 is annealed for 30 minutes at 900°C under an N₂ atmosphere in order to activate a dopant. Thereafter, a photoresist (not shown) is coated onto the polysilicon film 123 and photolithographically patterned. The polysilicon film 123 is further subjected to dry etching in accordance with anisotropic etching such as RIE (Reactive Ion Etching) to form the gate electrode 123a. Finally, a capacitor of a layered structure: a gate electrode - gate insulating film - a semiconductor substrate, was formed. Then, electric characteristics of the gate insulating film were examined by using the capacitor. In this embodiment, the gate electrode 123a is formed of polysilicon film 123, but the material of the gate electrode according to the present invention is never limited to a polysilicon, as being explained later. In the case that a device according to the present invention is actually fabricated, source/drain regions 124 are formed in the semiconductor substrate 121. However, in the case of examining the electric characteristics of gate insulating film, the formation of source/drain regions 124 is omitted since they are unnecessary in the above examination.

[0021] FIG. 3 shows the relation between a deposit temperature of a polysilicon film (gate electrode) and a film stress. In FIG. 3, the longitudinal axis indicates a film stress (MPa) of the polysilicon film on the semiconductor substrate, and the lateral axis indicates the film formation temperature (°C) of the polysilicon film. The polysilicon films were formed by deposited on the substrate in the same manner under the same conditions as in the aforementioned steps for manufacturing a capacitor, except the film formation temperature, that is, by varying the film formation temperature, and then annealing the polysilicon film, whereby obtaining various semiconductor wafers having capacitors of various electric characteristics. Thereafter, the stress of the polysilicon film alone was checked on the basis of warpage of the semiconductor wafer.

[0022] The stress of the polysilicon film itself was measured as follows.

[0023] Generally, compressive stress or tensile stress is generated in the polysilicon film, depending upon a deposition temperature of the polysilicon film. When the compressive stress is generated, "upward warpage" bent is produced, as shown in FIG. 4A. On the other hand, when the tensile stress is generated, "downward warpage" bent is produced, as shown in FIG. 4B. Hereinafter, the "upward warpage" bent will be expressed by a positive value, whereas the "downward warpage" bent by a negative value.

[0024] FIGS. 5A and 5B are conceptual views

showing how to obtain a warpage amount, arithmetically. FIG. 5A shows a state before the polysilicon film is deposited on a substrate. FIG. 5B shows a state after the polysilicon film is deposited on the substrate.

In the figures, reference symbol t_s denotes a thickness of a substrate, t_r is a thickness of the deposited film (polysilicon film), D is a diameter of the portion at which warpage is measured (corresponding to the warpage), and X is a warpage amount (μm).

[0025] The film stress σ may be arithmetically obtained in accordance with a general equation for stress:

$$\sigma = \frac{E_s}{6(1-\gamma_s)} \cdot \frac{(t_s)^2}{t_r} \cdot \frac{1}{r}$$

where σ is a film stress, E_s is a Young's modulus of a substrate (semiconductor wafer), and γ_s is a Poisson's ratio of the substrate.

[0026] Herein, from the following Equation I:

$$r = \frac{X^2 + (D/2)^2}{2X} \approx \frac{(D/2)^2}{2X} = \frac{D^2}{8X} \quad \because X \ll r \quad (I)$$

[0027] Equation II is deduced.

$$\sigma = \frac{E_s}{6(1-\gamma_s)} \cdot \frac{(t_s)^2}{t_r} \cdot \frac{1}{r} \approx \frac{E_s}{6(1-\gamma_s)} \cdot \frac{(t_s)^2}{t_r} \cdot \frac{8X}{D^2} \quad (II)$$

[0028] Accordingly, stress σ is obtained on the basis of the warpage amount X . As mentioned before, since a "upward warpage" is defined as a positive value, and a "downward warpage" a negative value, a film stress in the case of "upward warpage" has a positive value, while a film stress in the case of a "downward warpage" has a negative value.

[0029] The film stress of the polysilicon film alone is defined as the difference in warpage amount before and after the polysilicon film is deposited, as being illustrated in FIGS. 5A and 5B. The warpage amount is measured by using Flexsus FLX-2418 (manufactured by KLA Tencor Corporation), as a measuring device.

[0030] Referring again to FIG. 3, it has been found that the film stress is as small as 50 MPa (absolute value) or less at a deposition temperature of 700°C or more. As the film formation temperature decreases from 700°C, a compressive stress is expressed, while a tensile stress reaches as large as -300 MPa at near 620°C. On the other hand, the stress immediately after the polysilicon film is formed, is 100 MPa or less. This value does not so significantly differ from that obtained after the annealing.

[0031] FIG. 6 shows the results of a total charge amount Qbd of the gate insulating film measured under

an electric field of 12 MV/cm, in the MOS capacitor thus formed on the semiconductor substrate. Note that the total charge amount Qbd is defined as the total amount of electric charge passing through the capacitor per unit area when a plurality of capacitors formed in the same plane of the semiconductor wafer are measured and a failure rate thereof reaches 50%.

[0032] In the case where the film stress is smaller than -300 MPa, the total amount of the electric charge Qbd is about 15 C/cm². However, in the case where the film stress ranges from -200 MPa to about +30MPa, the total charge amount Qbd is as large as 25C/cm² or more. This means that the total charge amount of the gate insulating film 122 is 25C/cm² or more when the polysilicon film forming gate electrode 123a is formed at a film formation temperature of 640°C or more, preferably 650°C or more. In addition, in a preferable embodiment, the atmosphere pressure in depositing a polysilicon film serving as a gate electrode may be in a range of 20 to 200 Torr.

[0033] In this embodiment, a single-wafer processing LPCVD apparatus is used. In the present invention, however, a batch processing LPCVD apparatus usually employed in manufacturing a semiconductor device, may be used.

[0034] By using the batch processing LPCVD apparatus, the polysilicon film serving as the gate electrode was formed, at a temperature from 500°C to 630°C and a pressure from 0.3 Torr to 1 Torr while SiH₄ gas is supplied at a flow rate from 200 sccm to 1000 sccm. As a result, the polysilicon film formed at a temperature of 580°C or more was crystallized. At this time, the film stress was -300 MPa or less (300 MPa or less in terms of absolute value).

[0035] The results for the MOS capacitor manufactured by the batch processing LPCVD apparatus were the same as those of the MOS capacitor manufactured by the single-wafer processing LPCVD apparatus. That is, the total charge amount Qbd causing dielectric breakdown of the gate insulating film was about 15 C/cm². Furthermore, the silicon film deposited at a film formation temperature of 580°C or less is in an amorphous state and has a compressive film stress of about -300 MPa. The amorphous film is crystallized into a polysilicon film in the annealing step performed later. The film stress of the polysilicon film greatly increases to a tensile stress of about 300 MPa in absolute value. When such a polysilicon film is used, the total charge amount of the gate insulating film comes to about 15/cm². The MOS capacitor manufactured by the batch processing LPCVD apparatus satisfies the same relationship between the total charge amount Qbd of the gate insulating film and the film stress of the gate electrode shown in FIGS. 3 and 6.

[0036] The same results as in the aforementioned embodiment are given in the case where MOS capacitor having a polysilicon film doped with phosphorus (P) or boron (B) is used in place of the film doped with

arsenic (As). Furthermore, even if the concentration of the dopant is varied, the same results are obtained. Thus, it has been found that the film stress of a gate electrode is determined mainly by its film formation temperature, regardless of dopant materials or dopant concentration.

[0037] The gate insulating film of 8 nm thick is used in this embodiment. When the film thickness of the oxide film is changed, the total charge amount of the gate insulating film varies, accordingly. When the film thickness of the gate insulating film decreases, the total charge amount Qbd reduces, whereas when the film thickness increases, the total charge amount Qbd increases. However, the relationship between the film stress and the total charge amount of the gate insulating film is unchanged. That is, when the film stress of the gate electrode increases, the total charge amount of the gate insulating film decreases. To be more specific, when the film stress is 200 MPa or less, the total charge amount Qbd is about twice as large as that obtained at the film stress of 300 MPa.

[0038] In the case where the gate electrode is formed of another substance such as a metal including tungsten (W), the effect of the film stress upon the total charge amount Qbd of the gate insulating film is similar and thus, the same phenomenon is observed. Hence, when the metal electrode is used, it is effective to set the film stress of the gate electrode at 200 MPa or less in terms of absolute value, in order to improve the total charge amount Qbd of the gate insulating film, in other word, to improve reliability thereof.

[0039] Referring to FIG. 7, a second embodiment will be explained.

[0040] In the first embodiment, a single-wafer processing LPCVD apparatus is used. When the single-wafer processing LPCVD apparatus is heated at high temperatures, the formed film is sometimes degraded in uniformity in thickness. To maintain the uniformity of film thickness, the semiconductor wafer is rotated in the apparatus.

[0041] FIG. 7 is a schematic sectional view of the single-wafer processing LPCVD apparatus. As shown in the figure, the LPCVD apparatus has a reaction chamber (film formation chamber) 21. In the film formation chamber 21, a wafer holder 22 is provided for mounting a semiconductor wafer 24 thereon. The wafer holder 22 is designed so as to rotate at a predetermined rotation number to rotate the semiconductor wafer 24. The film formation chamber 21 has a heater 23 therein for heating an inner space during film formation time.

A reactive gas is supplied to the inner space of the film formation chamber 21 from a pipe 20 while being controlled by a mass-flow controller 27 and a valve 26. After completion of a reaction, an exhaust gas is discharged through a pipe 211 by a pump 210. The pump 210 is controlled by a valve 28 and a conductance valve 29.

[0042] A gas flow 25 of the reactive gas supplied through the pipe 20 enters from an upper portion of the

film formation chamber 21, passes through slits and is supplied uniformly over a surface of the semiconductor wafer 24 in rotation. After completion of a reaction, the gas flow 25 is discharged from the pipe 211.

[0043] A semiconductor wafer was placed in the single-wafer processing LPCVD apparatus thus constructed and a reactive gas flow was supplied uniformly over the surface of the semiconductor wafer while the semiconductor wafer was rotated at a high speed. In this manner, a polysilicon film was formed on a semiconductor wafer. When the polysilicon film was formed by supplying SiH_4 at a flow rate of 1 SLM, AsH_3 at a flow rate of 3 sccm under a pressure of 50 Torr, and N_2 at a flow rate of 30 SLM, while the semiconductor wafer was rotated at a rotation number of 3000 rpm, the resultant polysilicon film was excellent in uniformity ($\pm 3\%$ or less) in thickness within the semiconductor wafer surface plane at the film formation temperature ranging from 600°C to 900°C . In this case, the film stress of the polysilicon film satisfied the same relationship between the film formation temperature and the film stress shown in FIG. 3.

Then, MOS capacitors were formed on a semiconductor substrate and a total charge amount Qbd determining dielectric breakdown of the gate insulating films of the capacitors was examined and measured. The results are the same as shown in FIG. 6. That is, according to the second embodiment, it is possible to provide a semiconductor device having a highly liable gate insulating film, with keeping a very preferable uniformity in film thickness.

[0044] Now, referring to FIG. 8, a third embodiment will be explained.

[0045] FIG. 8 is a cross sectional view of an EEPROM memory cell according to the third embodiment of the invention. The EEPROM is a non-volatile electrically erasable and programmable memory, and mostly used in a new fields including a logic array capable of programming data memory and logic in a logic circuit, e.g., a micro computer, data memories, and program memories of IC cards.

[0046] As the semiconductor substrate, for example, a p-type semiconductor substrate 31 is used. The surface of the semiconductor substrate 31 is oxidized with O_2 , H_2O , or HCl gas at a temperature of 800°C to form a thermal oxide film 34 of 8 nm thick serving as a gate insulating film.

[0047] Thereafter, the semiconductor substrate 31 is placed as a semiconductor wafer in the film formation chamber of the LPCVD apparatus shown in FIG. 1. A polysilicon film 35 constituting a floating gate is formed on the semiconductor wafer of about 200 nm thick at a film formation temperature of 680°C while SiH_4 gas is supplied at a flow rate of 1 SLM and AsH_3 gas at 1 sccm under a pressure of 5 Torr. The film stress of polysilicon film 35 can be suppressed less than about 200 MPa in its absolute value by forming polysilicon film in the same manner as above the first embodiment or the second

embodiment. As a result the polysilicon film 35 constituting a floating gate can have a total charge amount Qbd as twice large as a conventional one, so that a semiconductor device having a highly liable floating gate can be provided.

[0048] At this time, arsenic (As) is introduced into the polysilicon film 35 in an amount of about 1×10^{20} atoms/ cm^3 . Thereafter, the polysilicon film 35 is annealed at 900°C for 30 minutes under a N_2 atmosphere in order to activate a dopant.

[0049] Subsequently, a photoresist (not shown) is coated onto the polysilicon film 35 and photolithographically patterned. The resultant polysilicon film 35 is etched by a RIE method to form a floating gate 35 of polysilicon. Then, an interlayer insulating film (SiO_2) film 36 is formed on the semiconductor wafer by a CVD method so as to cover the floating gate 35. Subsequently, a polysilicon film 37 is formed on the semiconductor wafer of about 200 nm thick, for example, in the LPCVD apparatus shown in FIG. 1, in the same conditions as in the formation time of the floating gate 35. At this time, Arsenic (As) is introduced into the polysilicon film 37 in an amount of about 1×10^{20} atoms/ cm^3 . Thereafter, the polysilicon film 37 is annealed at 900°C under a N_2 atmosphere in order to activate a dopant. Thereafter, a photoresist (not shown) is coated onto the polysilicon film 37 and photolithographically patterned. The polysilicon film 37 is etched by RIE to form a control gate 37 of polysilicon.

[0050] Note that the single-wafer processing LPCVD apparatus shown in FIG. 1 is used in this case, however, the polysilicon film forming the gate electrode may be formed in the single-wafer processing LPCVD apparatus shown in FIG. 7.

[0051] Then, n-type impurity ions such as boron are doped in the semiconductor substrate 31 by using the control gate 37 as a mask and thermally diffused to form an n^+ source region 32 and an n^+ drain region 33. Then, an insulating film (SiO_2) 38 is deposited by the CVD method on the semiconductor substrate 31 so as to cover the control gate 37. The surface of the insulating film 38 is planarized by a CMP (Chemical Mechanical Polishing) method. Then, a photoresist (not shown) is coated onto the insulating film 38 and photolithographically patterned. The resultant insulating film 38 is etched by RIE etc. to form a contact hole 38 through which the drain region 33 is exposed. Subsequently, an aluminium film 310 is deposited by a sputtering method on the insulating film 38 and within the contact hole 39, and photolithographically patterned to form a metal wiring 310.

[0052] As for the device such as EEPROM for writing data into a memory cell by using a tunnel current, the Qbd value is significant since it determines how many times the device can be programmed. Therefore, it is necessary to increase the total charge amount Qbd in order to improve the performance of the device. In the EEPROM in which the total amount Qbd of the electric

charge passing through the gate insulating film directly influences upon characteristics of a device, the number of times the device can be programmed or rewritten is greatly improved by the present invention. Since the film stress of the gate electrode according to the present invention is suppressed to 200 MPa or less in terms of absolute value, the total charge amount Qbd of the gate insulating film increases nearly double. As a result, the life spans of transistors and LSI products having the MOS structure increase double, increasing reliability of the device. This feature is particularly useful in EEPROM in which the total charge amount Qbd directly influences upon characteristics of a device, since the number of times the device can be programmed or rewritten increases approximately double.

Claims

1. A semiconductor device characterized by comprising:

a semiconductor substrate (121);
source/drain regions (124) formed on the semiconductor substrate;
a gate insulating film (122) formed between the source/drain regions on the semiconductor substrate; and
a gate electrode (123a) formed on the gate insulating film,
characterized in that:
a film stress of the gate electrode is 200 MPa or less in terms of absolute value.

2. The semiconductor device according to claim 1, characterized in that the gate electrode is in contact with the gate insulating film.

3. The semiconductor device according to claim 1, characterized in that the gate electrode is formed of a polysilicon film.

4. The semiconductor device according to claim 1, characterized in that the gate electrode comprises at least one of a metal silicide film and a high-melting point metal film.

5. The semiconductor device according to claim 4, characterized in that the high melting point metal film is formed on the metal suicide film

6. A non-volatile semiconductor device characterized by comprising:

a semiconductor substrate (31);
source/drain regions (32, 33) formed on the semiconductor substrate;
a gate insulating film (34) formed between the source/drain regions on the semiconductor

substrate; and

a floating gate (35) formed on the gate insulating film,
characterized in that
a film stress of the floating gate is 200 MPa or less in terms of absolute value.

7. A method of manufacturing a semiconductor device, comprising the steps of:

forming source/drain regions (124) in a semiconductor substrate (121);
forming a gate insulating film (122) between the source/drain regions of the semiconductor substrate; and forming a gate electrode (123a) formed of a polysilicon film on the gate insulating film;
characterized in that:
a film stress of the gate electrode is 200 MPa or less in terms of absolute value.

8. The method according to claim 7, characterized in that the gate electrode comprises a polysilicon film which is formed by depositing the gate insulating film by a CVD method at an atmosphere temperature of 640°C or more.

9. The method according to claim 8, characterized in that the atmosphere temperature is 650°C or more.

10. The method according to claim 8, characterized in that the step of forming the gate electrode includes a step of forming a polysilicon film while rotating the semiconductor substrate at a high speed.

11. The method according to claim 10, characterized in that the rotation speed is 3000 rpm or more in the step of forming a polysilicon film while rotating the semiconductor substrate.

12. The method according to claim 7, characterized in that the gate electrode is a floating gate.

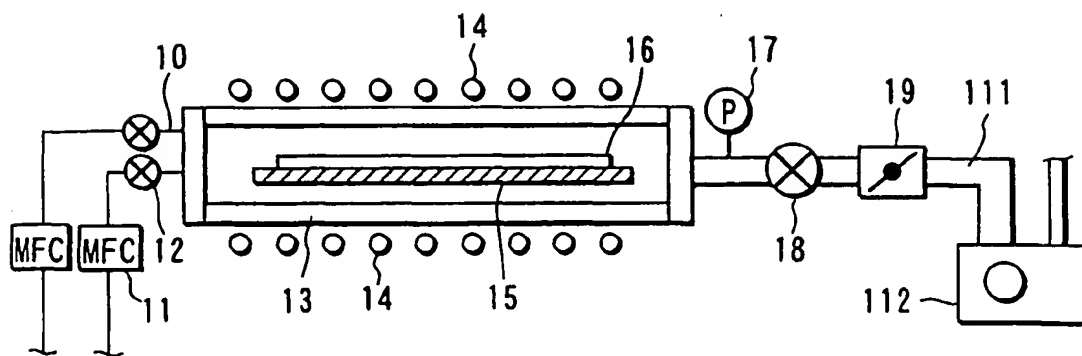


FIG. 1

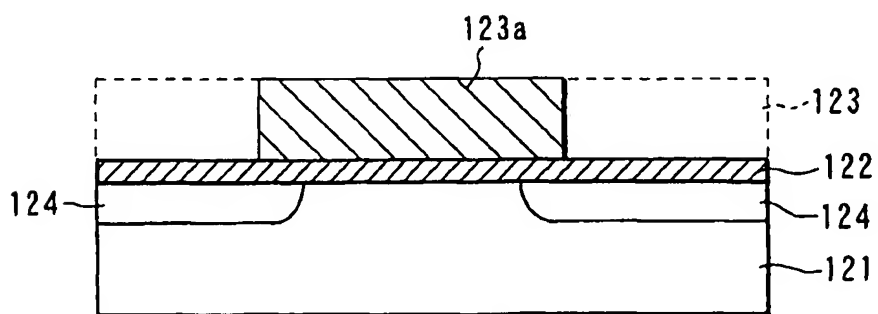


FIG. 2

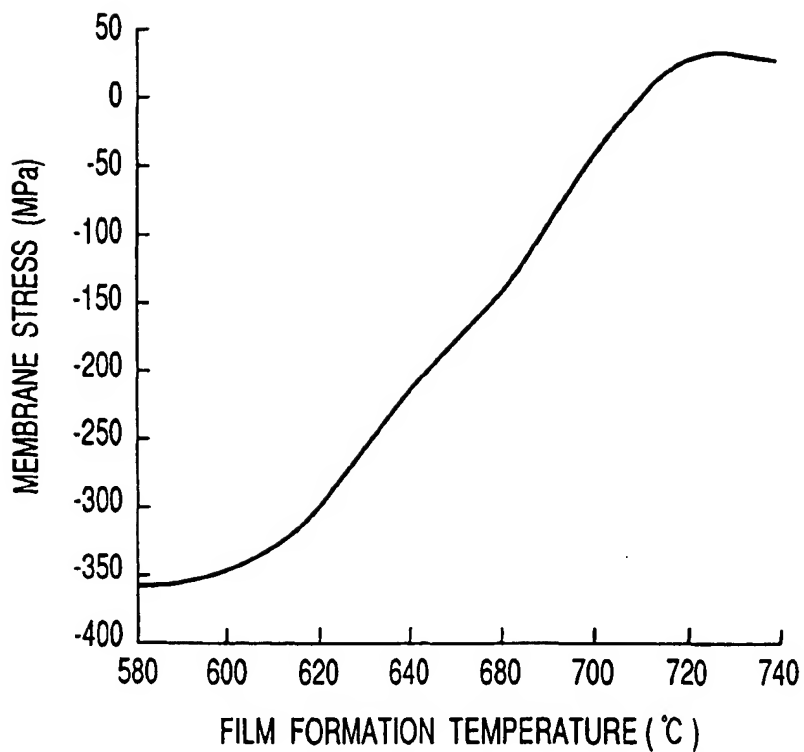


FIG. 3

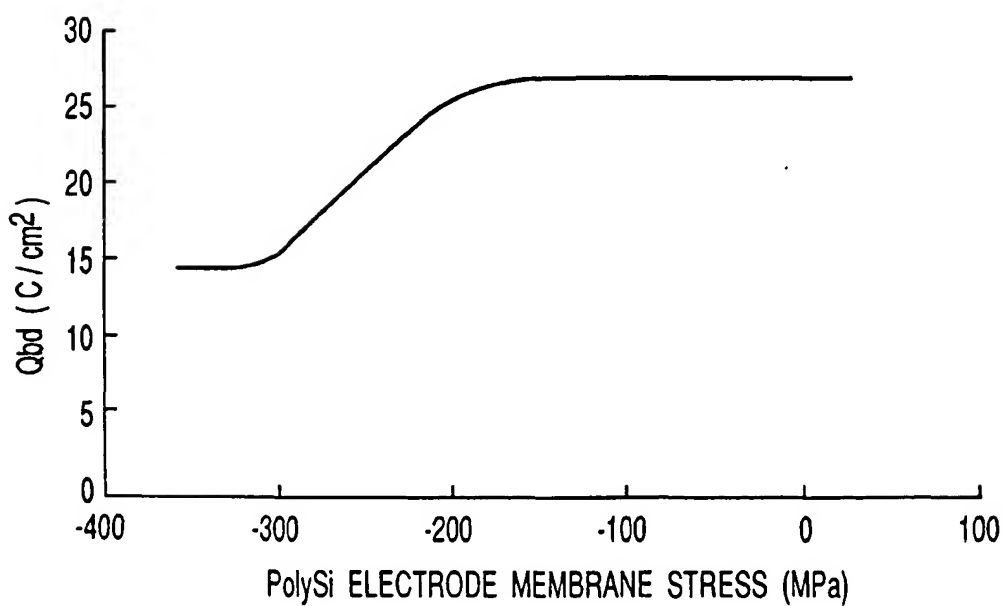


FIG. 6

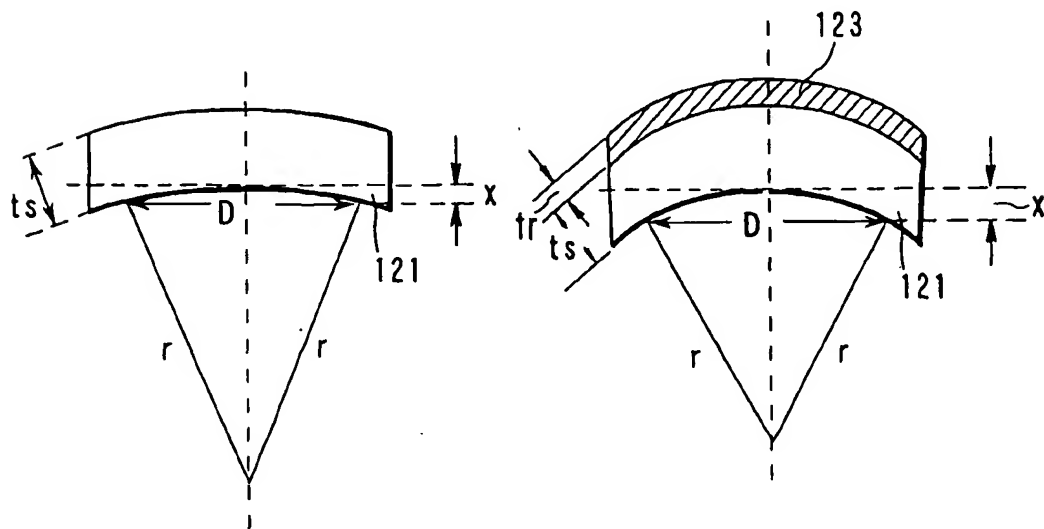
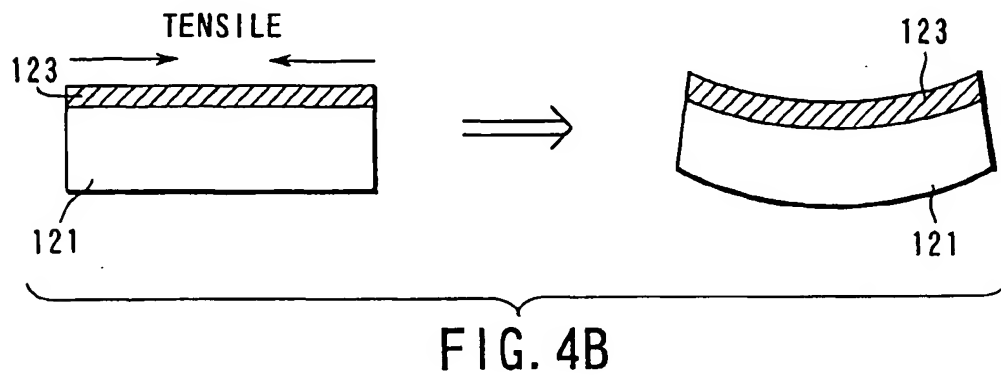
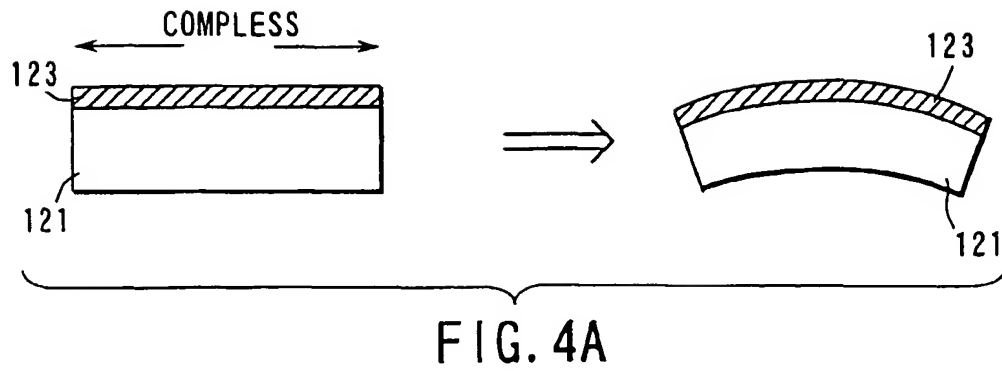


FIG. 5A

FIG. 5B

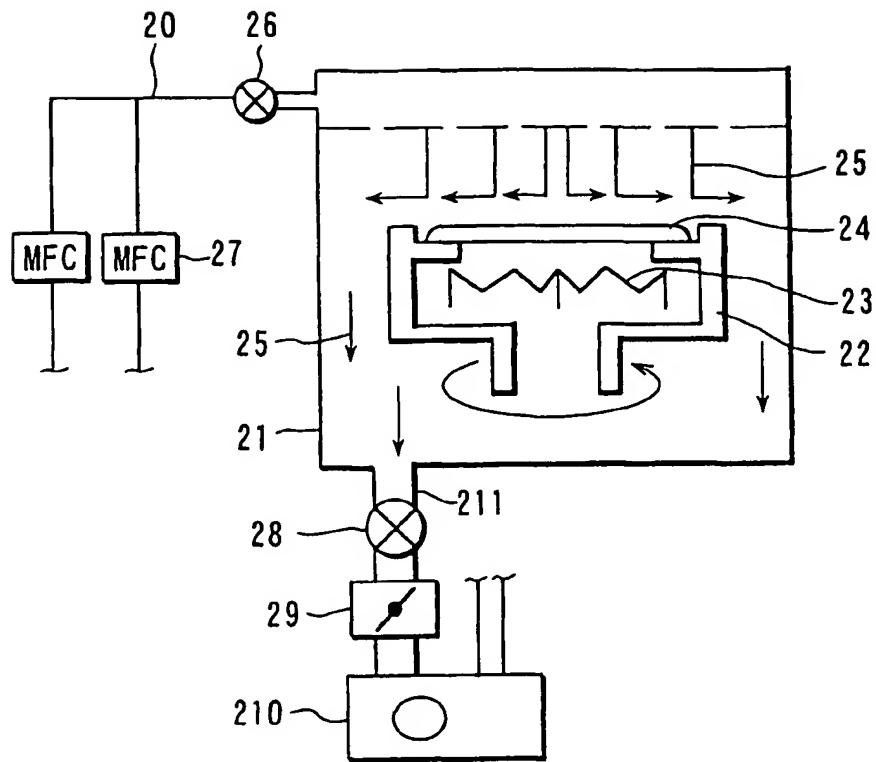


FIG. 7

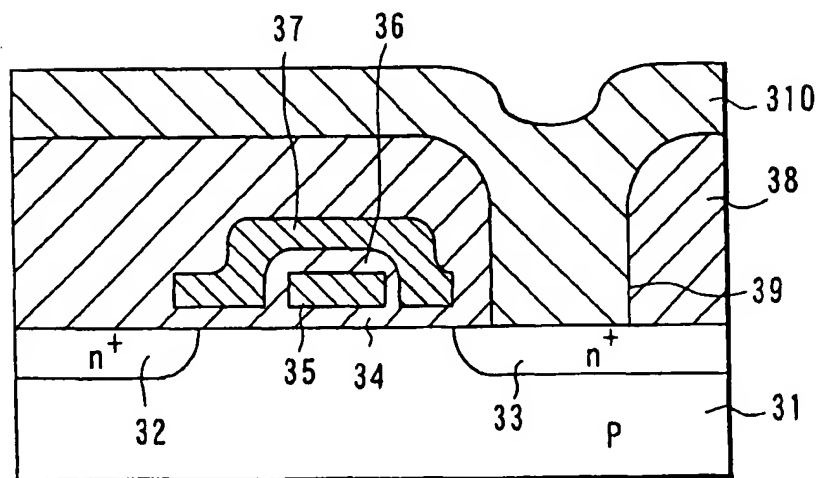


FIG. 8

